



1.5-Gbps LVDS/LVPECL/CML-TO-CML TRANSLATOR/REPEATER

FEATURES

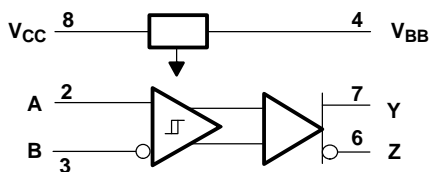
- Provides Level Translation From LVDS or LVPECL to CML, Repeating From CML to CML
- Signaling Rates⁽¹⁾ up to 1.5 Gbps
- CML Compatible Output Directly Drives Devices With 3.3-V, 2.5-V, or 1.8-V Supplies
- Total Jitter < 70 ps
- Low 100 ps (Max) Part-To-Part Skew
- Wide Common-Mode Receiver Capability Allows Direct Coupling of Input Signals
- 25 mV of Receiver Input Threshold Hysteresis Over 0-V to 4-V Common-Mode Range
- Propagation Delay Times, 800 ps Maximum
- 3.3-V Supply Operation
- Available in SOIC and MSOP Packages

APPLICATIONS

- Level Translation
- 622-MHz Central Office Clock Distribution
- High-Speed Network Routing
- Wireless Basestations
- Low Jitter Clock Repeater⁽¹⁾

(1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

FUNCTIONAL DIAGRAM



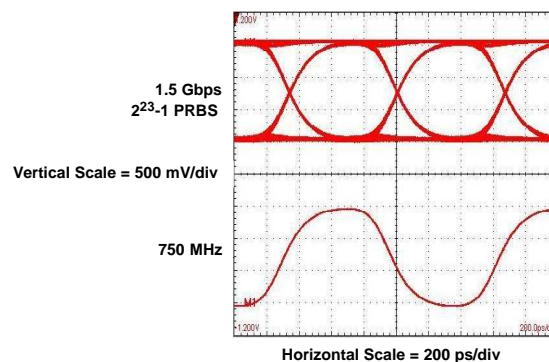
DESCRIPTION

This high-speed translator/repeater is designed for signaling rates up to 1.5 Gbps to support various high-speed network routing applications. The driver output is compatible with current-mode logic (CML) levels, and directly drives 50-Ω or 25-Ω loads connected to 1.8-V, 2.5-V, or 3.3-V nominal supplies. The capability for direct connection to the loads may eliminate the need for coupling capacitors. The receiver input is compatible with LVDS (TIA/EIA-644), LVPECL, and CML signaling levels. The receiver tolerates a wide common-mode voltage range, and may also be directly coupled to the signal source. The internal data path from input to output is fully differential for low noise generation and low pulse-width distortion.

The V_{BB} pin is an internally generated voltage supply to allow operation with a single-ended LVPECL input. For single-ended LVPECL input operation, the unused differential input is connected to V_{BB} as a switching reference voltage. When used, decouple V_{BB} with a 0.01-μF capacitor and limit the current sourcing or sinking to 400 μA. When not used, V_{BB} should be left open.

This device is characterized for operation from -40°C to 85°C.

EYE PATTERN



$V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, $|V_{ID}| = 200\text{ mV}$, $V_{IC} = 1.2\text{ V}$, $V_{TT} = 3.3\text{ V}$, $R_T = 50\ \Omega$



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

PART NUMBER	PART MARKING	PACKAGE	STATUS
SN65CML100D	CML100	SOIC	Production
SN65CML100DGK	NWB	MSOP	Production

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted⁽¹⁾

		UNIT	
V_{CC}	Supply voltage range ⁽²⁾	–0.5 V to 4 V	
I_{BB}	Sink/source	±0.5 mA	
	Voltage range, (A, B, Y, Z)	0 V to 4.3 V	
Electrostatic discharge	Human Body Model ⁽³⁾	A, B, Y, Z, and GND	±5 kV
		All pins	±2 kV
	Charged-Device Model ⁽⁴⁾	All pins	±1500 V
	Continuous power dissipation	See Dissipation Rating Table	
T_{stg}	Storage temperature range	–65°C to 150°C	
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C	

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
- (3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.7.
- (4) Tested in accordance with JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT	
V_{CC}	Supply voltage	3	3.3	3.6	V	
V_{TT}	Terminator supply voltage	3.3-V nominal supply at terminator	3	3.3	3.6	V
		2.5-V nominal supply at terminator	2.375	2.5	2.625	
		1.8-V nominal supply at terminator	1.7		1.9	V
$ V_{ID} $	Magnitude of differential input voltage	0.1		1	V	
	Input voltage (any combination of common-mode or input signals)	0		4	V	
V_{BB}	Output current			400	μA	
T_A	Operating free-air temperature	–40		85	°C	

PACKAGE DISSIPATION RATINGS

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ⁽¹⁾ ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ POWER RATING
DGK	425 mW	3.4 mW/°C	221 mW
D	725 mW	5.8 mW/°C	377 mW

- (1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

DEVICE CHARACTERISTICS

PARAMETER		MIN	NOM	MAX	UNIT
I_{CC}	Supply current, device only		9	12	mA
V_{BB}	Switching reference voltage ⁽¹⁾	1890	1950	2010	mV

(1) V_{BB} parameter varies 1:1 with V_{CC}

INPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold	See Figure 1 and Table 1				100	mV
V_{IT-}	Negative-going differential input voltage threshold			-100			
$V_{ID(HYS)}$	Differential input voltage hysteresis, $V_{IT+} - V_{IT-}$					25	mV
I_I	Input current (A or B inputs)	$V_I = 0$ V or 2.4 V, Second input at 1.2 V		-20			μ A
		$V_I = 4$ V, Second input at 1.2 V				33	
$I_{I(OFF)}$	Power off input current (A or B inputs)	$V_{CC} = 1.5$ V, $V_I = 0$ V or 2.4 V, Second input at 1.2 V		-20			μ A
		$V_{CC} = 1.5$ V, $V_I = 4$ V, Second input at 1.2 V				33	
I_{IO}	Input offset current ($ I_{IA} - I_{IB} $)	$V_{IA} = V_{IB}$, $0 \leq V_{IA} \leq 4$ V		-6			μ A
C_i	Differential input capacitance	$V_I = 0.4 \sin(4E6\pi t) + 0.5$ V				3	pF
		$V_{CC} = 0$ V				3	

(1) All typical values are at 25°C and with a 3.3-V supply.

OUTPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V_{OH}	Output high voltage ⁽²⁾	$R_T = 50$ Ω , $V_{TT} = 3$ V to 3.6 V or $V_{TT} = 2.5$ V $\pm 5\%$, See Figure 2		$V_{TT}-60$	$V_{TT}-10$	V_{TT}	mV
V_{OL}	Output low voltage ⁽²⁾			$V_{TT}-1100$	$V_{TT}-800$	$V_{TT}-640$	mV
$ V_{OD} $	Differential output voltage magnitude			640	780	1000	mV
V_{OH}	Output high voltage ⁽³⁾	$R_T = 25$ Ω , $V_{TT} = 3$ V to 3.6 V or $V_{TT} = 2.5$ V $\pm 5\%$, See Figure 2		$V_{TT}-60$	$V_{TT}-10$	V_{TT}	mV
V_{OL}	Output low voltage ⁽³⁾			$V_{TT}-550$	$V_{TT}-400$	$V_{TT}-320$	mV
$ V_{OD} $	Differential output voltage magnitude			320	390	500	mV
V_{OH}	Output high voltage ⁽²⁾	$R_T = 50$ Ω , $V_{TT} = 1.8$ V $\pm 5\%$, See Figure 2		$V_{TT}-170$	$V_{TT}-10$	V_{TT}	mV
V_{OL}	Output low voltage ⁽²⁾			$V_{TT}-1100$	$V_{TT}-800$	$V_{TT}-640$	mV
$ V_{OD} $	Differential output voltage magnitude			570	780	1000	mV
V_{OH}	Output high voltage ⁽³⁾	$R_T = 25$ Ω , $V_{TT} = 1.8$ V $\pm 5\%$, See Figure 2		$V_{TT}-85$	$V_{TT}-10$	V_{TT}	mV
V_{OL}	Output low voltage ⁽³⁾			$V_{TT}-500$	$V_{TT}-400$	$V_{TT}-320$	mV
$ V_{OD} $	Differential output voltage magnitude			285	390	500	mV
C_o	Differential output capacitance	$V_I = 0.4 \sin(4E6\pi t) + 0.5$ V				3	pF
		$V_{CC} = 0$ V				3	

(1) All typical values are at 25°C and with a 3.3-V supply.

(2) Outputs are terminated through 50- Ω resistors to V_{TT} ; CML level specifications are referenced to V_{TT} and tracks 1:1 with variation of V_{TT} .

(3) Outputs are terminated through 25- Ω resistors to V_{TT} ; CML level specifications are referenced to V_{TT} and tracks 1:1 with variation of V_{TT} .

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM ⁽¹⁾	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$R_T = 50 \Omega$ or $R_T = 25 \Omega$, See Figure 4	250		800	ps
t_{PHL}	Propagation delay time, high-to-low-level output		250		800	ps
t_r	Differential output signal rise time (20%–80%)				300	ps
t_f	Differential output signal fall time (20%–80%)				300	ps
$t_{sk(p)}$	Pulse skew ($ t_{PHL} - t_{PLH} $) ⁽²⁾			0	50	ps
$t_{sk(pp)}$	Part-to-part skew ⁽³⁾	$V_{ID} = 0.2 V$			100	ps
$t_{jit(per)}$	Period jitter, rms (1 standard deviation) ⁽⁴⁾	750 MHz clock input ⁽⁵⁾		1	5	ps
$t_{jit(cc)}$	Cycle-to-cycle jitter (peak) ⁽⁴⁾	750 MHz clock input ⁽⁶⁾		8	27	ps
$t_{jit(pp)}$	Peak-to-peak jitter ⁽⁴⁾	1.5 Gbps 2 ²³ -1 PRBS input ⁽⁷⁾		30	70	ps
$t_{jit(det)}$	Deterministic jitter, peak-to-peak ⁽⁴⁾	1.5 Gbps 2 ⁷ -1 PRBS input ⁽⁸⁾		25	65	ps

- (1) All typical values are at 25°C and with a 3.3-V supply.
- (2) $t_{sk(p)}$ is the magnitude of the time difference between the t_{PLH} and t_{PHL} .
- (3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
- (4) Jitter parameters are ensured by design and characterization. Measurements are made with a Tektronix TDS6604 oscilloscope running Tektronix TDSJIT3 software. Agilent E4862B stimulus system jitter 2 ps $t_{jit(per)}$, 16 ps $t_{jit(cc)}$, 25 ps $t_{jit(pp)}$, and 10 ps $t_{jit(det)}$ has been subtracted from the values.
- (5) $V_{ID} = 200 mV$, 50% duty cycle, $V_{IC} = 1.2 V$, $t_r = t_f \leq 25 ns$ (20% to 80%), measured over 1000 samples.
- (6) $V_{ID} = 200 mV$, 50% duty cycle, $V_{IC} = 1.2 V$, $t_r = t_f \leq 25 ns$ (20% to 80%).
- (7) $V_{ID} = 200 mV$, $V_{IC} = 1.2 V$, $t_r = t_f \leq 0.25 ns$ (20% to 80%), measured over 100k samples.
- (8) $V_{ID} = 200 mV$, $V_{IC} = 1.2 V$, $t_r = t_f \leq 0.25 ns$ (20% to 80%). Deterministic jitter is sum of pattern dependent jitter and pulse width distortion.

PARAMETER MEASUREMENT INFORMATION

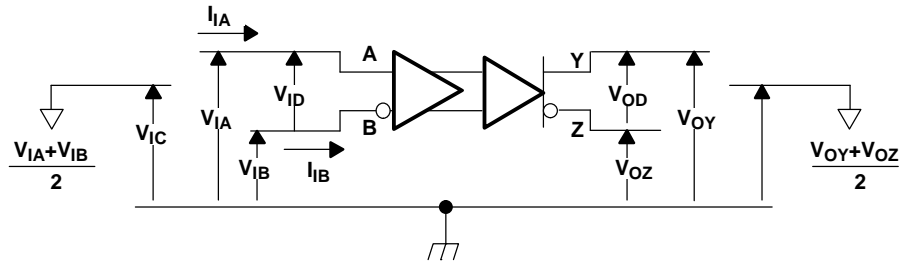


Figure 1. Voltage and Current Definitions

Table 1. Maximum Receiver Input Voltage Threshold

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE	OUTPUT ⁽¹⁾
V _{IA}	V _{IB}	V _{ID}	V _{IC}	
1.25 V	1.15 V	100 mV	1.2 V	H
1.15 V	1.25 V	-100 mV	1.2 V	L
4.0 V	3.9 V	100 mV	3.95 V	H
3.9 V	4.0 V	-100 mV	3.95 V	L
0.1 V	0.0 V	100 mV	0.5 V	H
0.0 V	0.1 V	-100 mV	0.5 V	L
1.7 V	0.7 V	1000 mV	1.2 V	H
0.7 V	1.7 V	-1000 mV	1.2 V	L
4.0 V	3.0 V	1000 mV	3.5 V	H
3.0 V	4.0 V	-1000 mV	3.5 V	L
1.0 V	0.0 V	1000 mV	0.5 V	H
0.0 V	1.0 V	-1000 mV	0.5 V	L

(1) H = high level, L = low level

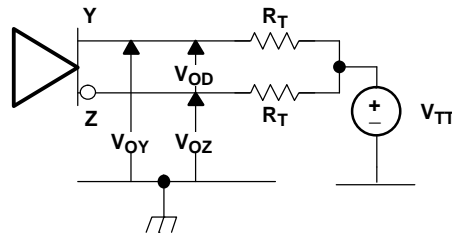


Figure 2. Output Voltage Test Circuit

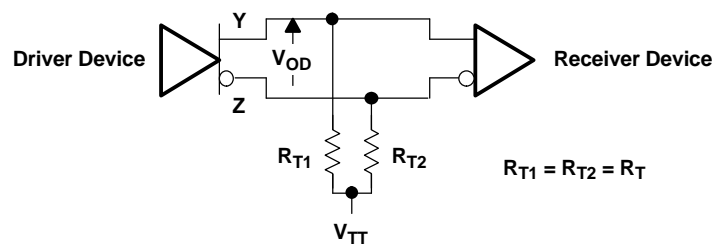
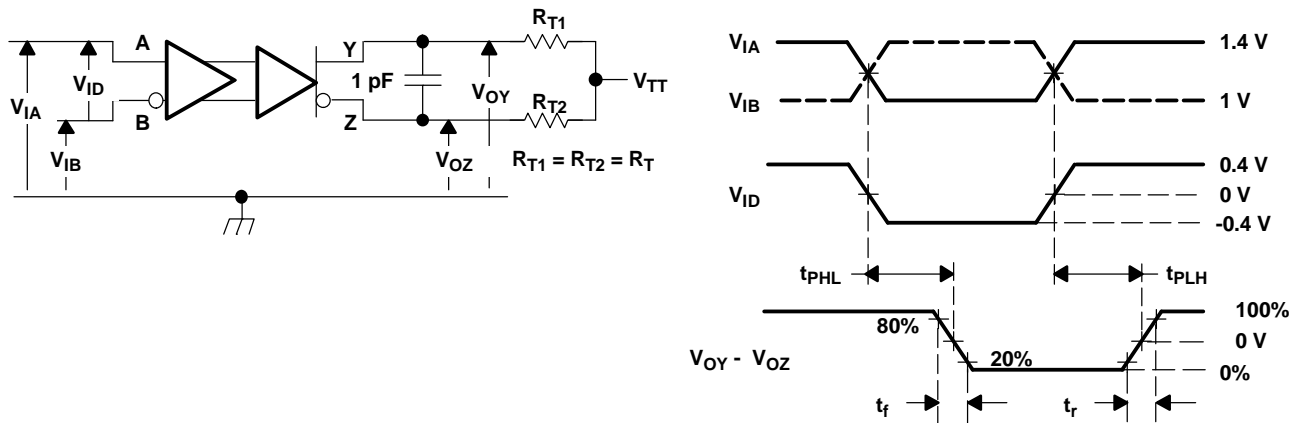


Figure 3. Typical Termination for Output Driver



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 0.25$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T. Measurement equipment provides a bandwidth of 5 GHz minimum.

Figure 4. Timing Test Circuit and Waveforms

PIN ASSIGNMENTS

D AND DGK PACKAGE
(TOP VIEW)

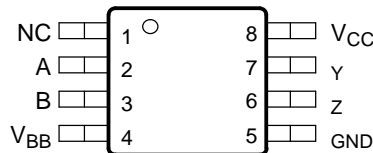


Table 2. PIN DESCRIPTIONS

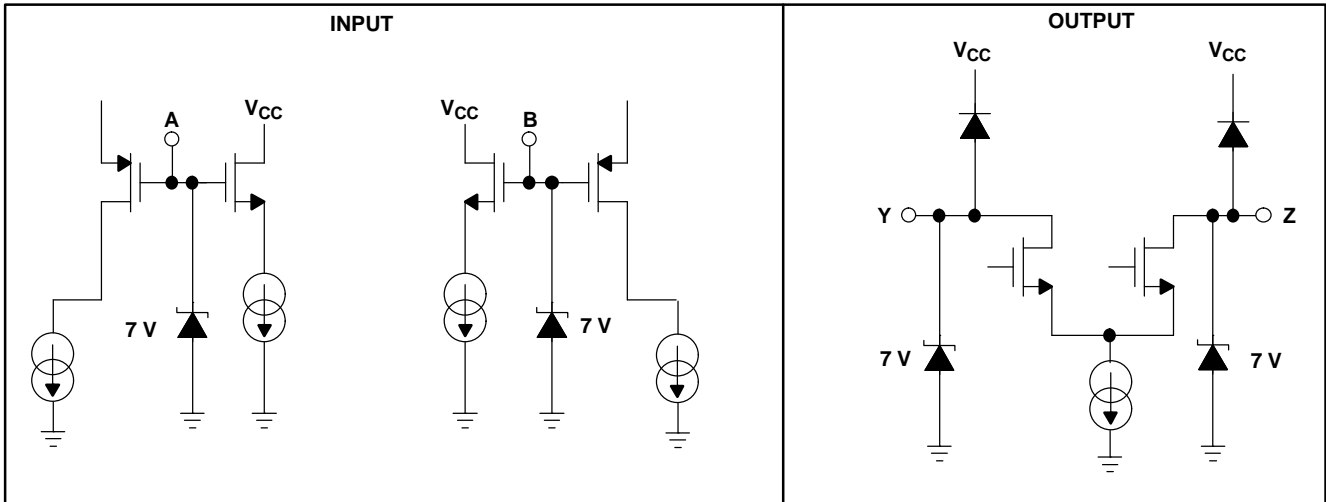
PIN	FUNCTION
A, B	Differential inputs
Y, Z	Differential outputs
V_{BB}	Reference voltage output
V_{CC}	Power supply
GND	Ground
NC	No connect

Table 3. FUNCTION TABLE

DIFFERENTIAL INPUT	OUTPUTS ⁽¹⁾	
$V_{ID} = V_A - V_B$	Y	Z
$V_{ID} \geq 100$ mV	H	L
-100 mV $< V_{ID} < 100$ mV	?	?
$V_{ID} \leq -100$ mV	L	H
Open	?	?

(1) H = high level, L = low level, ? = intermediate

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



TYPICAL CHARACTERISTICS

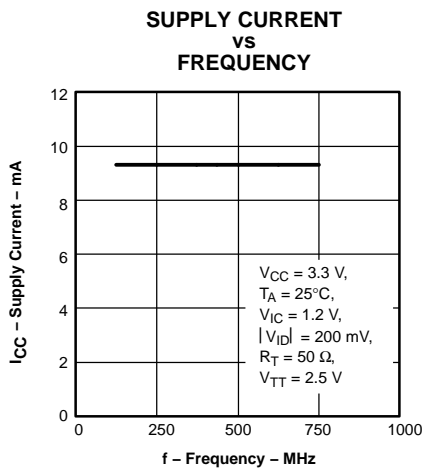


Figure 5.

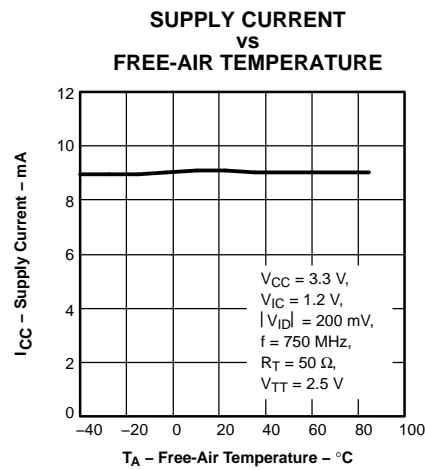


Figure 6.

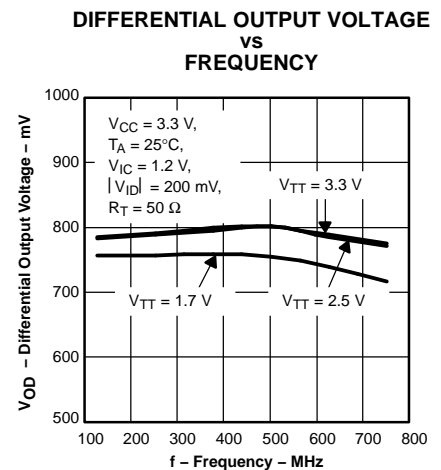


Figure 7.

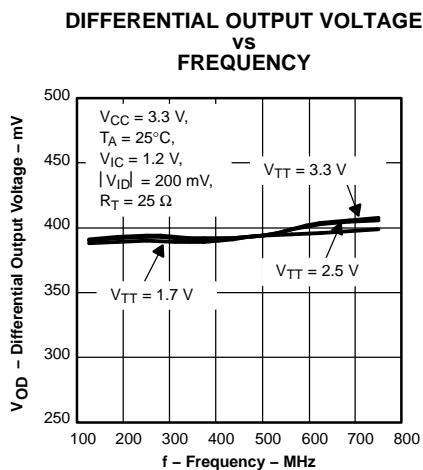


Figure 8.

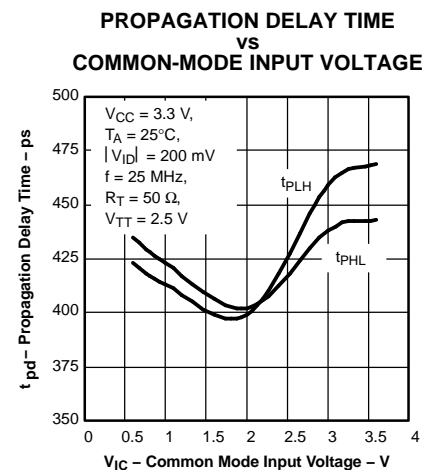


Figure 9.

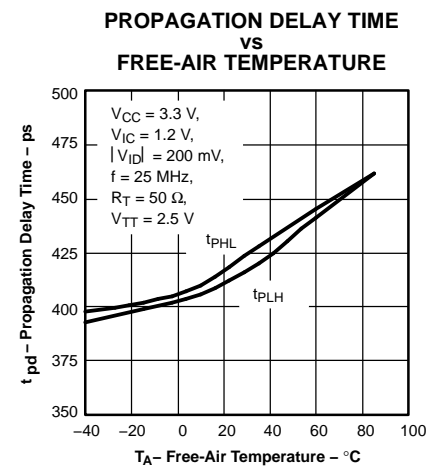


Figure 10.

TYPICAL CHARACTERISTICS (continued)

PROPAGATION DELAY TIME
VS
FREE-AIR TEMPERATURE

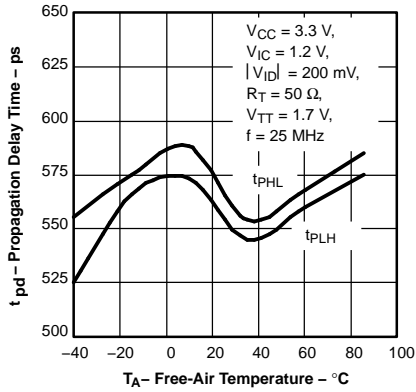


Figure 11.

PEAK-TO-PEAK JITTER
VS
FREQUENCY

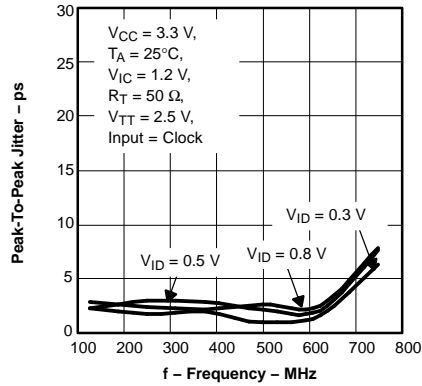


Figure 12.

PEAK-TO-PEAK JITTER
VS
DATA RATE

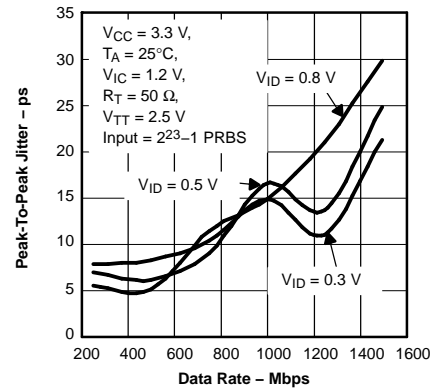


Figure 13.

PEAK-TO-PEAK JITTER
VS
COMMON MODE INPUT VOLTAGE

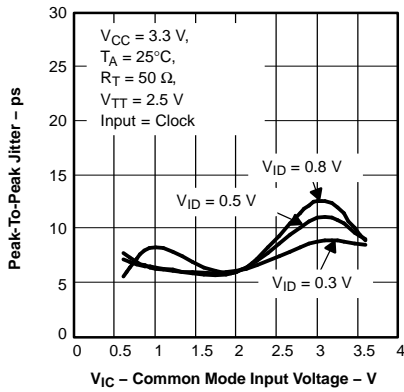


Figure 14.

PEAK-TO-PEAK JITTER
VS
COMMON MODE INPUT VOLTAGE

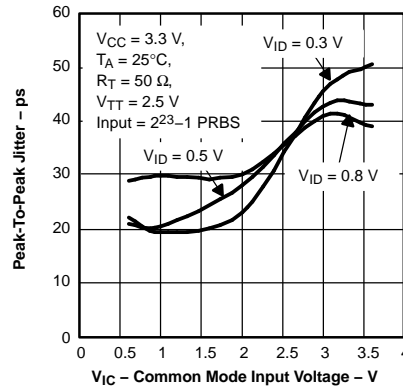


Figure 15.

PEAK-TO-PEAK JITTER
VS
DATA RATE

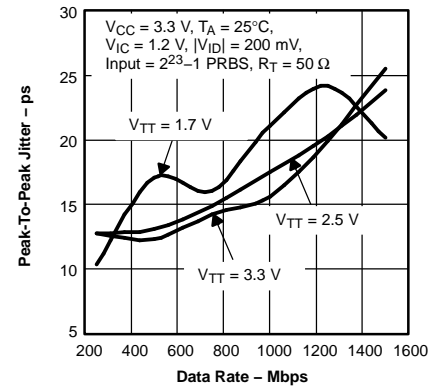


Figure 16.

PEAK-TO-PEAK JITTER
VS
DATA RATE

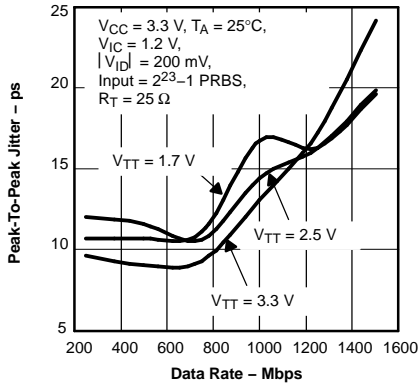
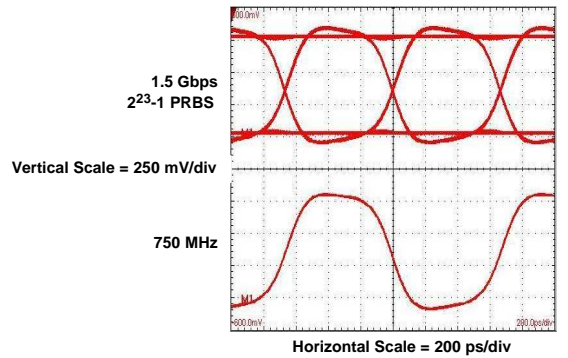


Figure 17.



V_{CC} = 3.3 V, T_A = 25°C, |V_{ID}| = 200 mV, V_{IC} = 1.2 V, V_{TT} = 3.3 V, R_T = 25 Ω

Figure 18.

TYPICAL CHARACTERISTICS (continued)

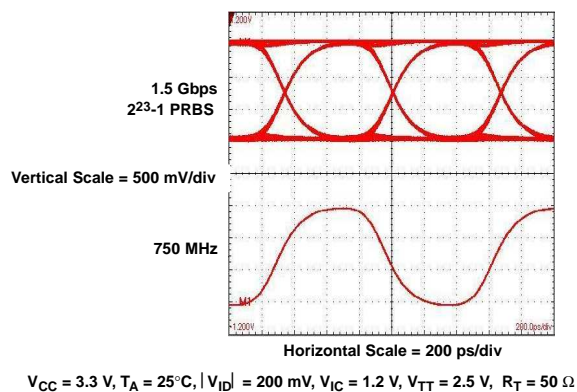


Figure 19.

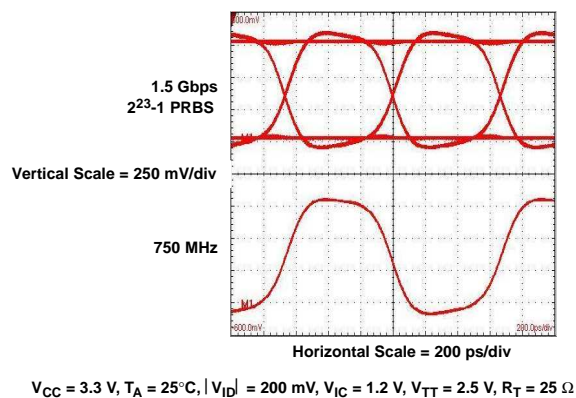


Figure 20.

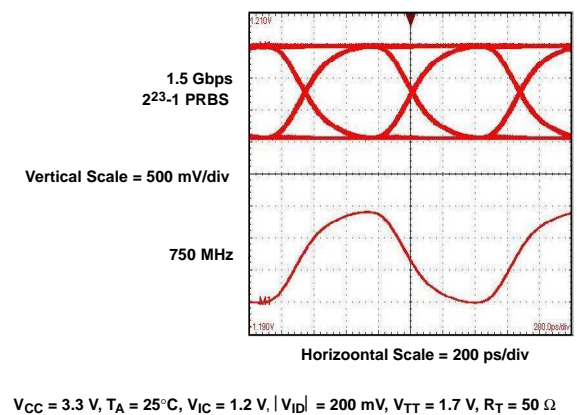


Figure 21.

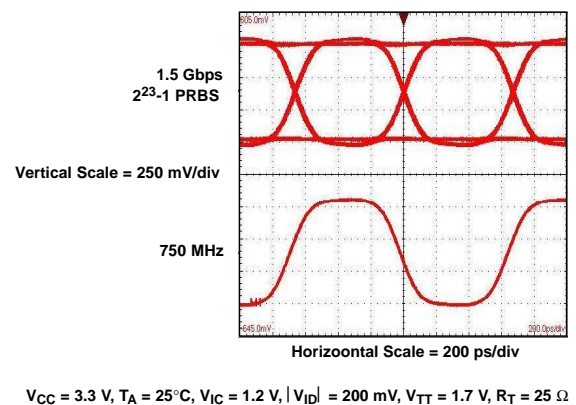


Figure 22.

TYPICAL CHARACTERISTICS (continued)

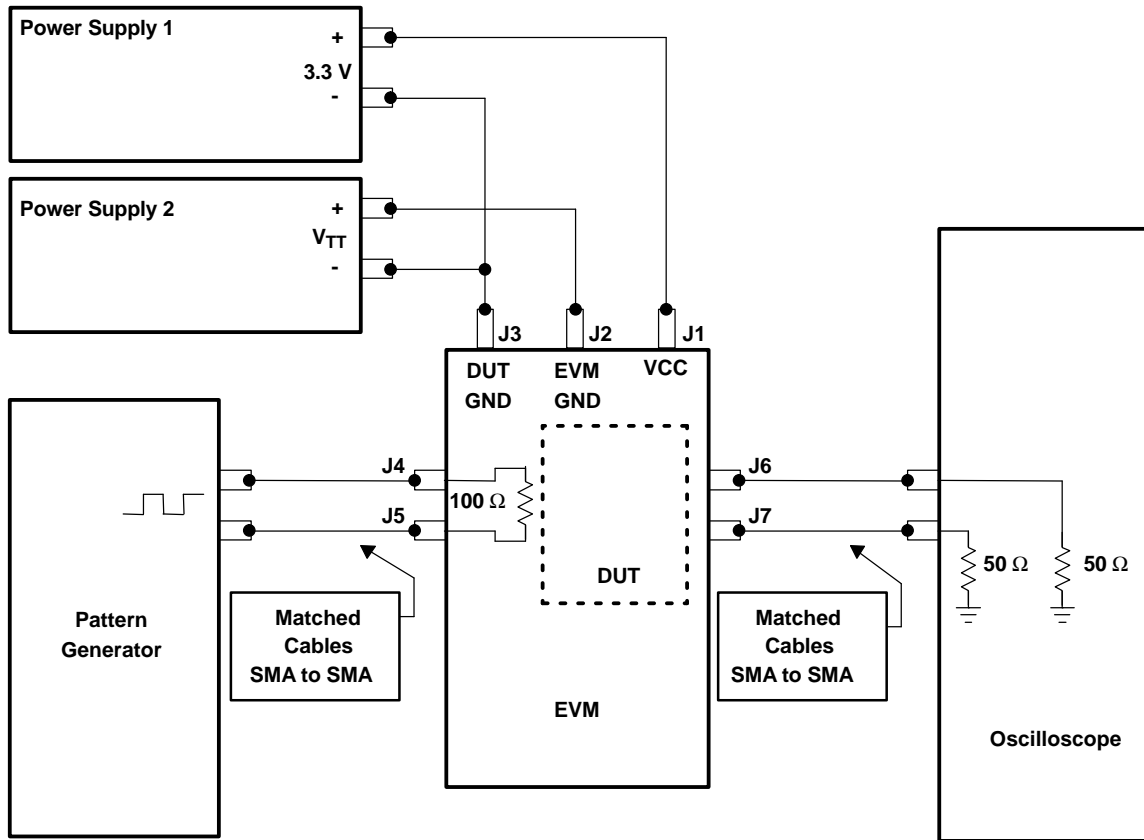


Figure 23. Jitter Setup Connections for SN65CML100

APPLICATION INFORMATION

For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. When V_{BB} is used, decouple V_{BB} via a 0.01- μF capacitor and limit the current sourcing or sinking to 0.4 mA. When not used, V_{BB} should be left open.

TYPICAL APPLICATION CIRCUITS (ECL, PECL, LVDS, etc.)

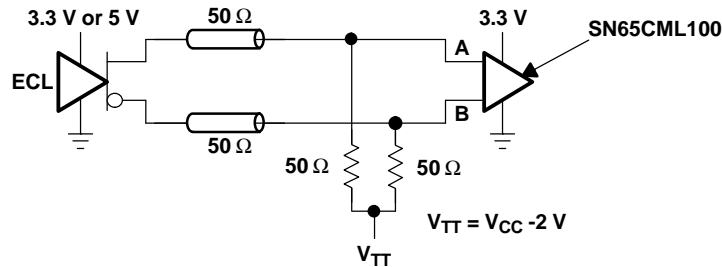


Figure 24. Low-Voltage Positive Emitter-Coupled Logic (LVPECL)

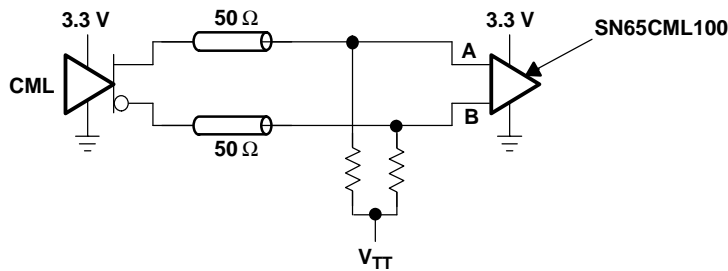


Figure 25. Current-Mode Logic (CML)

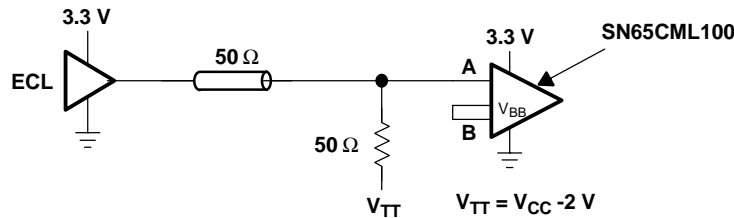


Figure 26. Single-Ended (LVPECL)

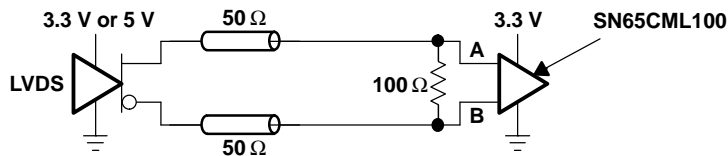


Figure 27. Low-Voltage Differential Signaling (LVDS)

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN65CML100D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65CML100DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65CML100DGK	ACTIVE	MSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65CML100DGKG4	ACTIVE	MSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65CML100DGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65CML100DGKRG4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65CML100DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65CML100DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

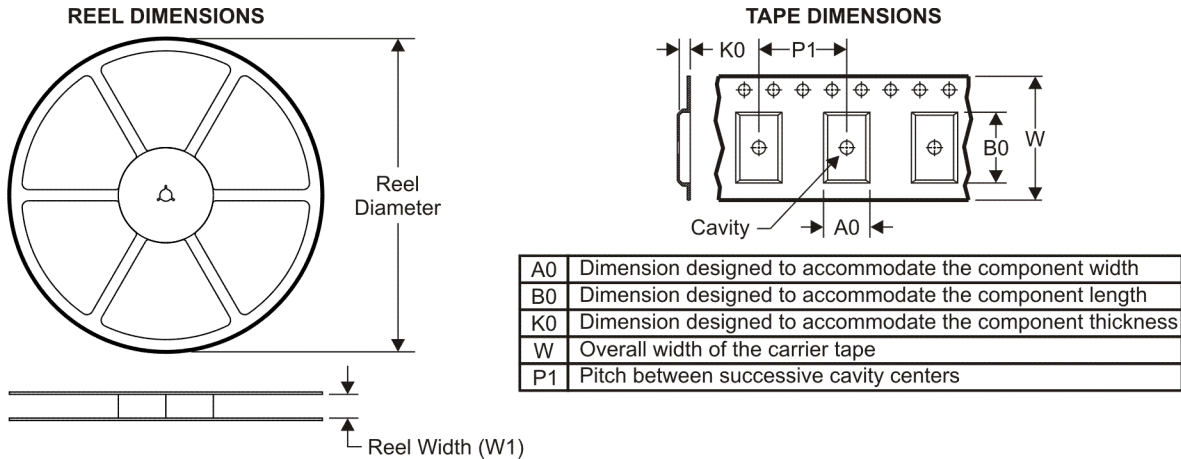
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



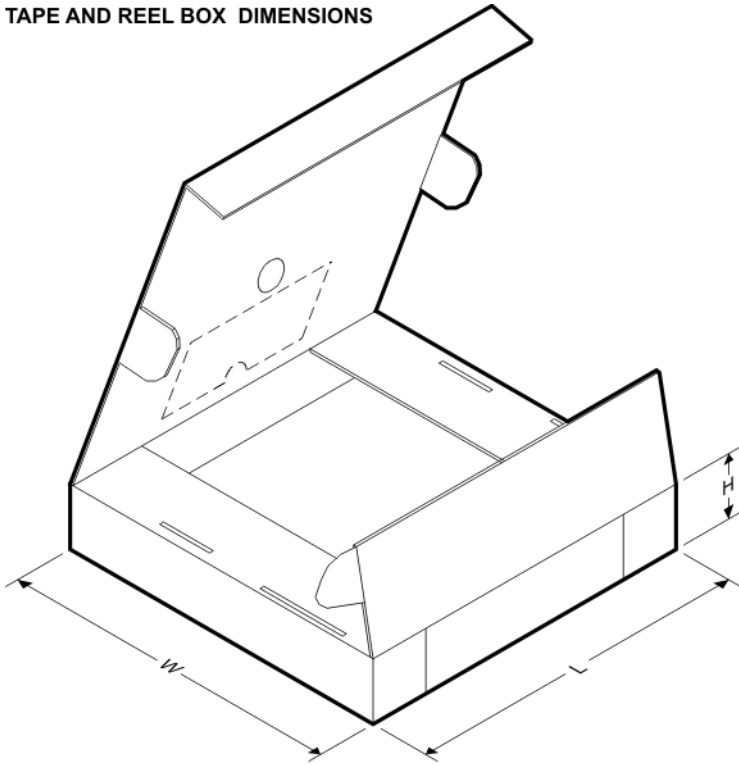
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65CML100DGKR	MSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65CML100DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

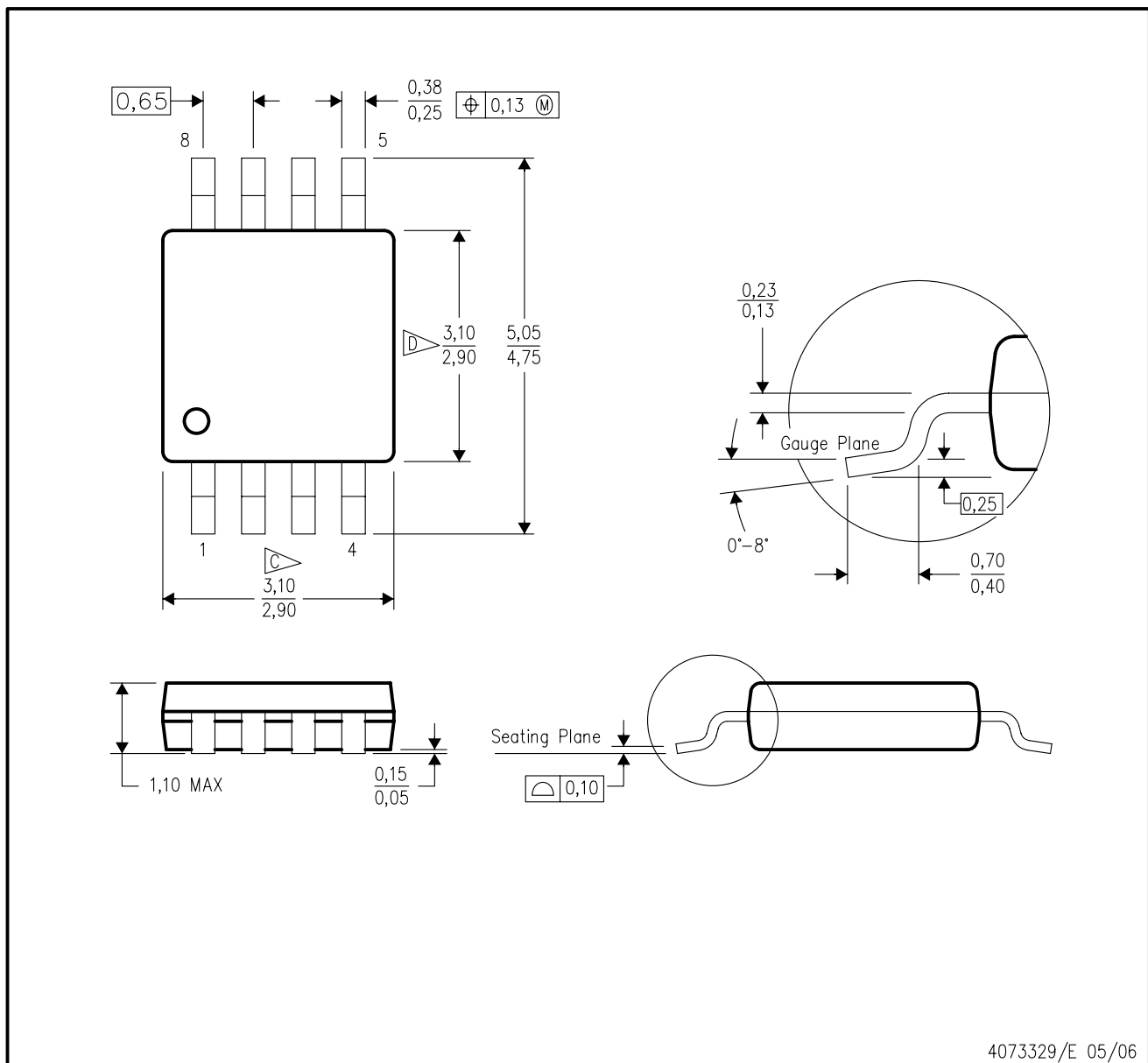


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65CML100DGKR	MSOP	DGK	8	2500	358.0	335.0	35.0
SN65CML100DR	SOIC	D	8	2500	346.0	346.0	29.0

DGK (S-PDSO-G8)

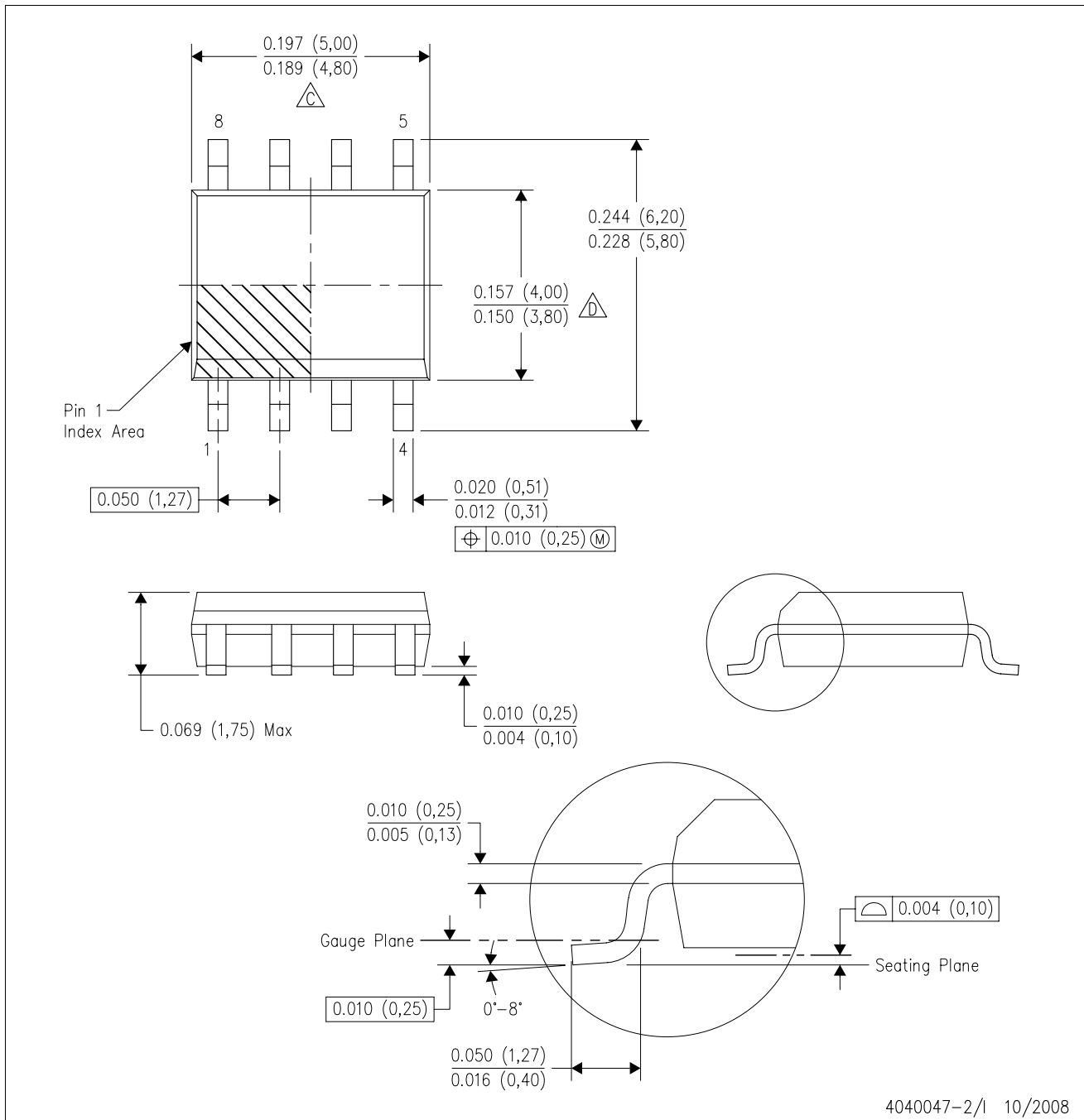
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
 - E. Falls within JEDEC MO-187 variation AA, except interlead flash.

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AA.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2008, Texas Instruments Incorporated